

LMX4169

Radio Transceiver for DECT

General description

The LMX4169 is a radio transceiver integrated circuit optimized for the Digital Enhanced Cordless Telecommunications (DECT) system. The transceiver, when combined with a power amplifier and a Tx/Rx switch, implements a complete DECT radio transceiver compliant with the ETSI CTR6 standard. The LMX4169 interfaces to National Semiconductor's SC144XX DECT family of baseband processors.

The LMX4169 integrates a complete transmitter, consisting of a phase locked loop, VCO and PA driver. The receiver contains LNA, quadrature downconverter, polyphase filter/combiner, automatic gain control, and demodulator.

The LMX4169 operates from a single 2.5V supply. The LMX4169 is manufactured in National's 0.25µm CMOS technology, and is packaged in a 44 pin LLP package.

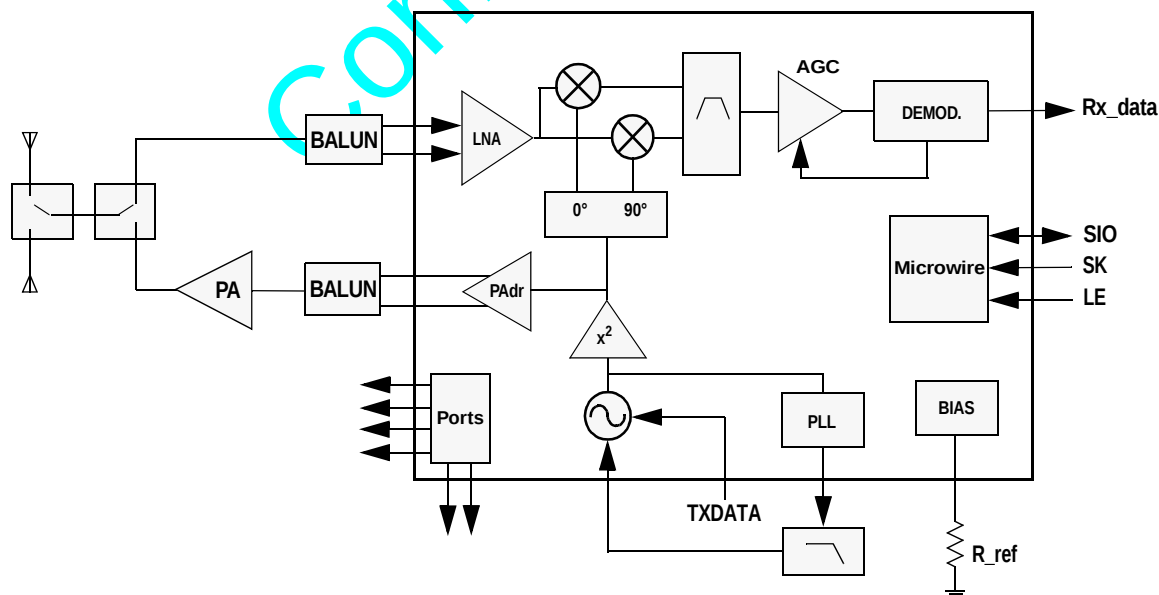
Features

- Highly integrated 1.9 GHz low-IF CMOS transceiver
- Down conversion to half the DECT channel spacing (864 kHz)
- On-chip channel select filter
- On-chip Voltage Controlled Oscillator (VCO)
- On-chip low noise amplifier (LNA)
- Open-loop modulation
- On-chip timing control
- Six digital output ports (including two for Antenna Diversity)
- +2 dBm PA driver RF output
- -96 dBm receiver sensitivity
- 2.5V operation
- Small 44 pin Leadless Leadframe Package

Applications

- (DECT) Digital Enhanced Cordless Telecommunications

System diagram



Note: MICROWIRE™ is a trademark of National Semiconductor Corporation

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1.0 Connection diagram

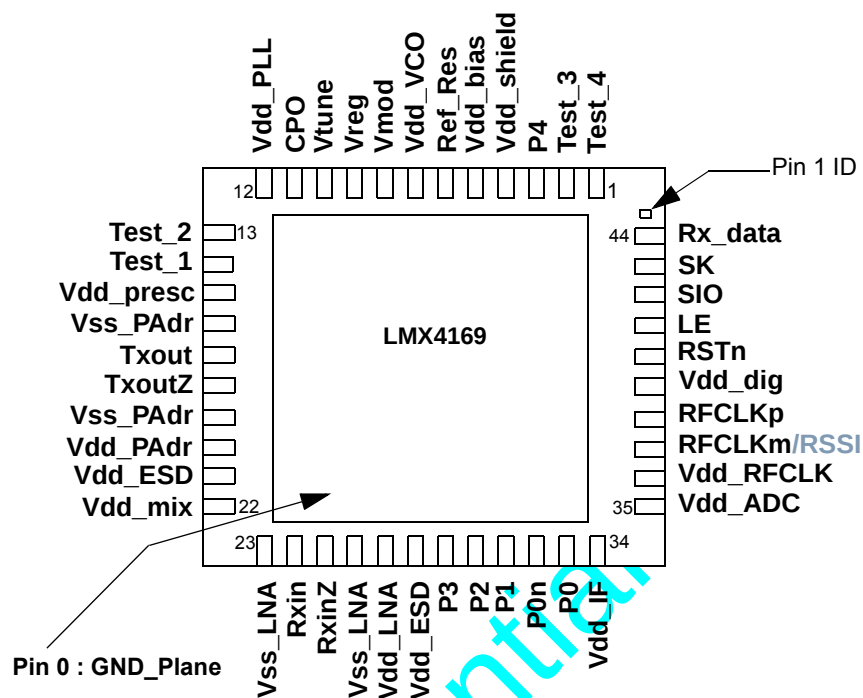


Figure 1 Connection diagram

Order Numbers:
 LMX4169ALQ (Note 1)
 NS Package Number LQA44 (see page 36)

Note 1: Refer to datasheet MS200164 for Surface Mount -Tape & Reel information.

This document can be downloaded from <http://www.national.com/ms/MS/MS200164-MISC.pdf>

2.0 Pin description

Table 1: Pin description

Pin Name	No.	Type	Reset state	Description	Equivalent I/O circuits
GND_Plane	0	-		Common ground	
Test_4	1	O	Hi-Z	Used for test purposes only. Must be connected to ground when not used	
Test_3	2	O	Hi-Z	Used for test purposes only. Must be connected to ground when not used.	
P4	3	O	Hi-Z	CMOS output	
Vdd_shield	4	-		Supply voltage	
Vdd_bias	5	-		Supply voltage	
Ref_Res	6	-		Connection for bias resistor R_ref (62 kΩ)	
Vdd_VCO	7	O		Supply voltage	
Vmod	8	I		VCO modulation input. Must be DC biased (preferably at Vdd/2) while the synthesizer is enabled and not modulated.	
Vreg	9	O		VCO voltage regulator output for decoupling purposes only	
Vtune	10	I		VCO frequency control input	
CPO	11	O		Charge Pump Output	
Vdd_PLL	12	-		Supply voltage	

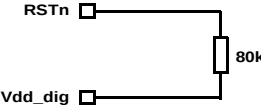
Table 1: Pin description

Pin Name	No.	Type	Reset state	Description	Equivalent I/O circuits
Test_2	13	-		Complementary external Local Oscillator input. Must be connected to ground when not used.	
Test_1	14	-		External Local Oscillator input. Must be connected to ground when not used.	
Vdd_presc	15	-		Supply voltage	
Vss_PAdr	16	-		Ground	
TxoutZ	17	O		Complementary PA driver output	
Txout	18	O		PA driver output	
Vss_PAdr	19	-		Ground	
Vdd_PAdr	20	-		Supply voltage	
Vdd_ESD	21	-		Supply voltage	
Vdd_mix	22	-		Supply voltage	

Table 1: Pin description

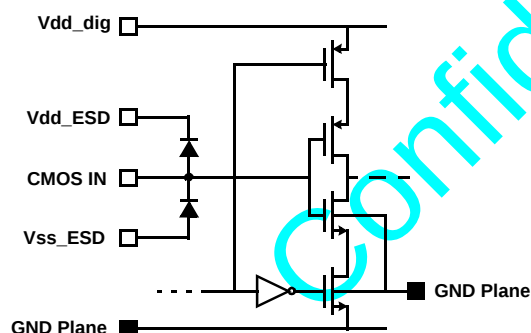
Pin Name	No.	Type	Reset state	Description	Equivalent I/O circuits
Vss_LNA	23	-		Ground	
Rxin	24	I		Receiver input. Must be AC coupled.	
RxinZ	25	I		Complementary receiver input. Must be AC coupled.	
Vss_LNA	26	-		Ground	
Vdd_LNA	27	-		Supply voltage	
Vdd_ESD	28	-		Supply voltage	
P3	29	O	Hi-Z	CMOS output	
P2	30	O	Hi-Z	CMOS output	
P1	31	O	Hi-Z	CMOS output	
P0n	32	O	Hi-Z	CMOS output (timing of P1/P2 in RX/TX mode, see Section 4.4)	
P0	33	O	Hi-Z	CMOS output (timing of P1/P2 in RX/TX mode, see Section 4.4)	
Vdd_IF	34	-		Supply voltage	
Vdd_ADC	35	-		Supply voltage	
Vdd_RFCLK	36	-		Supply voltage	
RFCLKm/ RSSI	37	I/O		Analog reference clock input or analog Receive Signal Strength Indicator output	
RFCLKp	38	I		Analog or Digital reference clock input (10.368 MHz)	

Table 1: Pin description

Pin Name	No.	Type	Reset state	Description	Equivalent I/O circuits
Vdd_dig	39	-		Digital supply pin	
RSTn	40	I		Reset. Active low CMOS input.	
LE	41	I		Microwire latch enable input. CMOS input, see paragraph 2.1.1.	
SIO	42	I/O		Microwire data input/output. CMOS input, see paragraph 2.1.1.	
SK	43	I		Microwire clock input. CMOS input, see paragraph 2.1.1.	
Rx_data	44	O		Data output to the baseband-controller. CMOS output, see paragraph 2.1.2.	

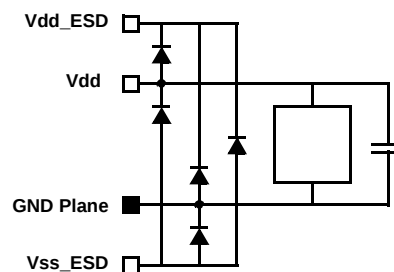
2.1 EQUIVALENT CIRCUITS

2.1.1 CMOS INPUT

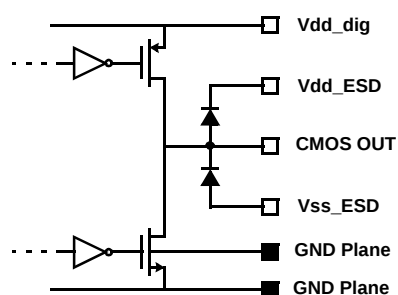


2.1.3 SUPPLY

(All Vdd_xxx, except Vdd_LNA, Vdd_PAdr and Vdd_shield).



2.1.2 CMOS OUTPUT



3.0 Introduction

3.1 FUNCTION AND OPERATION

The LMX4169 is designed to perform the complete receive function in a DECT receiver without requiring an external SAW filter at IF. Furthermore, the device includes a PLL and a VCO used for performing both transmit and receive functions. The device is designed to operate the frequency synthesizer in an open loop configuration both during transmit and receive.

The operation of LMX4169 can be divided into three distinct operations:

1. Set-up of the desired functionality,
2. Locking the frequency synthesizer, and
3. Performing the desired transmit or receive function.

All functions are controlled by programming the MICROWIRE™ interface of the device.

Before reception of a data slot, the frequency synthesizer is locked to the desired frequency. When locked, the PLL is tri-stated and the receive functions are switched on automatically.

Before transmission of a data slot, the frequency synthesizer is locked to the programmed frequency. When locked, the PLL is tri-stated and transmission is started automatically. The frequency synthesizer is designed to operate at half the desired frequency.

During receive, the signal at the input RF frequency is downconverted directly to an IF of 864kHz. At IF, blocking signals and noise are attenuated and the wanted signal is amplified to a sufficient level using an AGC amplifier. Thereafter the signal is demodulated, and the data is recreated along with an RSSI signal.

3.2 FREQUENCY SYNTHESIZER

The LMX4169 includes a PLL and a fully integrated VCO with an automatic tuning mechanism. The VCO is phase locked using the PLL and provides its output signal to a frequency doubler. The PLL requires an external loop filter.

3.2.1 PLL

The PLL includes a 12-bit N-counter implemented using a dual modulus 8/9 prescaler, and a 5 bit R-counter. The reference clock RFCLK may be provided as an analog differential or a digital single ended signal, see document **National Semiconductor Application Note AN-D-088**: "Interfacing the LMX4169 with the SC14430" for more information. A comparator is applied automatically in case the analog mode is chosen. The digital mode can be enforced, in which case the RFCLKm input becomes an analog RSSI output. The PLL contains a high performance charge pump with low leakage output when put in tri-state mode for open loop modulation. The charge pump current can be programmed by MICROWIRE™.

3.2.2 VCO

The VCO is fully integrated and has an automatic calibration mechanism to offset fabrication tolerances. Calibration is initiated using MICROWIRE™ control. The VCO is powered by an internally regulated supply.

3.2.3 Frequency Doubler

A frequency doubler is implemented in order to allow the VCO to run at a different frequency than the incoming/outgoing RF signal frequency and hence prevent load pulling due to activation of the PA.

3.3 RADIO RECEIVER

The receiver consists of an LNA and a quadrature downconversion mixer converting the desired channel to IF. At IF the signal is filtered and an Automatic Gain Control circuit adjusts the gain to allow the full dynamic range of the receiver to be utilized. After the amplification, the signal is converted to the digital domain and is demodulated.

3.3.1 LNA

The on board LNA is a fully differential structure integrated with the mixer providing low noise performance and good immunity from blocking signals.

3.3.2 Mixer

The mixer is an image reject type mixer. The mixer includes a phase shifting circuit required for quadrature signal generation.

3.3.3 Polyphase Filter

The polyphase filter recombines the quadrature signal and provides the required channel selectivity. The filter also serves as an anti-aliasing filter for the ADC which is part of the demodulator.

3.3.4 IF Amplifier

The gain controlled IF amplifier automatically adapts the wanted signal to the maximum input range of the demodulator.

3.3.5 AGC

A digitally realized automatic gain control is implemented to control the gain of the IF amplifiers.

3.3.6 Demodulator

The demodulator consists of an ADC and digital circuitry. Digital signal processing is used to extract the phase from the IF signal. The derivative of the phase over one symbol results in the demodulated data symbol. Automatic frequency control is used to maintain good sensitivity for IF frequency offsets up to +/-100kHz.

3.4 RADIO TRANSMITTER

During transmit the PLL output is tri-stated to a high impedance level and the VCO is modulated by a gaussian shaped data signal from the baseband IC (open loop modulation). The modulated output of the VCO is doubled in order to upconvert to the required transmit frequency.

3.5 PA DRIVER

The RF transmit output is differential and typically connected to the antenna via a power amplifier and a Tx/Rx switch. The PA driver provides a suitable output level to drive external PA circuitry.

3.6 MICROWIRE™ INTERFACE

The LMX4169 register set can be accessed through the MICROWIRE™ interface. To program the device, a data word is clocked into the shift register of this interface. Digital RSSI information is also available.

3.7 DIGITAL CONTROLLER

A digital controller is implemented in order to control the chip by timed control sequences. The timed control sequences will be defined by programming register banks. Two groups of control sequences can be defined. One for the receive mode and one for the transmit mode of the chip. By use of a control word (programmed via microwire), the chip is brought into either the receive or the transmit mode. Dependent on the mode indicated by the control word, one of the two groups of control sequences is started.

3.8 DIGITAL OUTPUT PORTS

Four logic output ports are available for general switching purposes. The signals provided at the ports can be used to control a Tx/Rx switch and/or the Power Amplifier. The logic level and the relative timing of the logic signals at the ports can be programmed by MICROWIRE™. Two additional ports (P0 and P0n) are meant for Antenna Diversity switching.

4.0 Microwire™ interface

4.1 MICROWIRE FUNCTIONALITY

The LMX4169 register set can be accessed through the MICROWIRE™ interface.

MICROWIRE™ is a three-wire serial interface to transfer data and control words from the baseband IC to the LMX4169 (by means of a **write** operation) and back (by means of a **read** operation).

A Microwire transaction consists of 24 bits (or 8 bits, see Section 4.2):

- The first bit (RW) discriminates between a read (RW = 1) and a write (RW = 0) operation.
- The next 7 bits (A6 to A0) are the address bits A[6:0].
- The final 16 bits (D15 to D0) are the data bits D[15:0].

The three wires of the interface are:

- LE: latch enable. This is an input to the LMX4169. All serial communication with the device is enabled only when this pin is high. When writing, the transferred information is decoded and stored into one of the on-chip registers on the falling edge of LE (no other clock is necessary to be active).
- SK: serial clock. This input controls the bit transfer rate. On the rising edge of SK, incoming serial data is clocked into the Microwire shift register. This signal has only effect when LE is high.
- SIO: data in/data out. This signal carries the bits transferred.

The timing of a write operation is shown in Figure 2 while the diagram for a read operation is given in Figure 3. Note that the read operation has half a clock cycle shift for the data bits.



Figure 2 Microwire write timing.

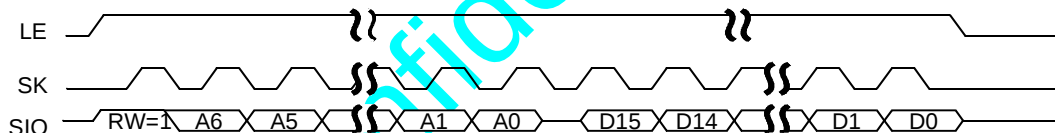


Figure 3 Microwire read timing.

Information on the interface of the LMX4169 with the baseband IC SC14430 can be found in a separate document: **National Semiconductor Application Note AN-D-088: "Interfacing the LMX4169 with the SC14430"**.

The 7 bits in the address word define a potential space of 128 registers with a width of 16 bits. The registers defined in this address space are presented in detail in Section 6. Registers having readable fields can be read as a whole; the others are write-only. Reading a write-only register results in returning value 0x5555. When reading a register with readable fields, the non-existing fields will be zero and the write-only fields will contain the written value.

For write-only registers, the distinction between address and data bits is not essential. Two registers of the LMX4169 are identified by 5 address bits A[6:2] and contain therefore 18 data bits (A[1:0] + D[15:0]). These are BURST_MODE_CONTROL_REG (see Section 4.2) and ALW_EN_REG (see Section 4.3). They have been designed in this way to optimize data transfer from a baseband IC.

4.2 BURST-MODE CONTROL WORD

Writing to the special 18-bit register BURST_MODE_CTRL_REG initiates most of the activities related to processing a TX or Rx slot. In particular, the **dynamic control functions**, the behavior of which can be configured in advance by static register settings (see Section 4.3) are activated by means of a single MICROWIRE™ transaction.

BURST_MODE_CTRL_REG is also called **burst-mode control word** (BMCW) for historical reasons.

For the BMCW, the information in A[1:0] should be interpreted as follows:

- A[0] = TX: 'transmit'; each time a '1' is written, the IC will initiate the processing of a "TX slot" and activate those blocks associated with transmitting according to a programmable sequence.
- A[1] = RX: 'receive'; each time a '1' is written, the IC will initiate the processing of an "Rx slot" and activate those blocks associated with receiving accord-

ing to a programmable sequence.

- When both A[0] and A[1] are '1', an autonomous IF-filter calibration procedure is executed in the hardware (see Section 5.2).

A BMCW transfer may consist of 8 bits only (LE falls after 8 rather than 24 bits). If 24 bits are sent, the data bits contain various settings that are likely to change from slot to slot (see Table 8).

4.3 DYNAMIC CONTROL FUNCTIONS

When the LMX4169 needs to process a transmit or receive slot, various blocks on the IC will be activated in some specific order according to programmable timing settings. The settings related to one block define the block's **dynamic control function** (DCF).

A DCF is characterized by a time instant when activation starts and an instant when activation terminates. These instants are specified relative to seven so-called switch instants (SIs). They are listed in Table 2. Each of them, except SO_SLOT which is fixed to time 0, can be programmed with a value between 0 and 1984 DECT bit periods, in multiples of 8. The values are programmed in the registers EO_CAL_RSSI_REG, TX_SI_REG and RX_SI_REG. The values are programmed as the actual switch instant in DECT bit periods divided by 8 (= 8 most significant bits). The offsets from the SIs can be specified using a granularity of a single DECT bit period within a range of 0 to 63.

Table 3: List of DCFs

DCF	description	controlled by	start SI	stop SI
PADRV	power-amplifier driver	TX or TRX ¹⁾²⁾	SO_TRX ³⁾	EO_TRX ⁴⁾
LNAMIX	low-noise amplifier and mixer	RX	SO_RX	EO_RX
LNAW	LNA window	RX	SO_RX	SO_RX
IF	intermediate-frequency filter	RX	SO_RX	EO_RX
ADC	analog-to-digital converter	RX	SO_RX	EO_RX
DEM	demodulator	RX	SO_RX	EO_RX
RSSIPH	RSSI peak-hold computation	RX	SO_RX	EO_RSSI or EO_RX ⁵⁾
DBL	frequency doubler	TRX	SO_TRX	EO_TRX
BIAS	bias circuit	TRX	SO_SLOT	EO_TRX
VCO	voltage-controlled oscillator	TRX	SO_SLOT	EO_TRX
VCOCORE	VCO core bias	TRX	SO_SLOT	EO_TRX
PLLCLOSED	PLL closed loop	TRX	SO_SLOT	SO_TRX or SO_TX/EO_RX ⁶⁾
COARSECAL	coarse calibration circuitry	TRX	SO_SLOT	none ⁷⁾
VCOFILTER	VCO core-bias-current filtering	TRX	EO_CAL	EO_TRX
PORT1 PORT2 PORT3 PORT4	general-purpose output ports	TX, RX or TRX ⁸⁾	SO_TRX	EO_TRX
FAD_WINDOW	fast antenna diversity window	RX	SO_RX	SO_RX

Table 2: List of switch instants

switch instant	description
SO_SLOT	start of slot (fixed at time 0)
EO_CAL	end of calibration (programmable)
EO_RSSI	end of RSSI measurement (programmable)
SO_TX	start of transmit (programmable)
SO_RX	start of receive (programmable)
EO_TX	end of transmit (programmable)
EO_RX	end of receive (programmable)

The SIs with respect to which the programmable set and reset times are specified, are hardwired. In addition, the control of activation by either TX, RX or either of the two is hardwired as well. For each DCF , there is a register _DCF_REG. The DCFs and their associated SIs are listed in Table 3. The registers have the following fields (port DCFs are slightly different and are discussed later on):

- SET_OFFSET: limited-range offset in DECT bit periods for the start time of the DCF measured from start SI.
- RESET_OFFSET: limited-range offset in DECT bit periods for the stop time of the DCF measured from stop SI.
- DIS: disable block activation.

- 1) TRX is the Boolean OR of TX and RX.
- 2) The sensitivity of PADRV for either TX or TRX is determined by a control bit (see PADRV_RCDF_REG).
- 3) SO_TRX means SO_TX when in a TX slot and SO_RX when in an RX slot.
- 4) EO_TRX means EO_TX when in a TX slot and EO_RX when in an RX slot.
- 5) The stop SI becomes EO_RX when BURST_MODE_CTRL_REG[RSSI_STOP_AT_RX] = 1.
- 6) When PLL_CTRL_REG[PLL_CLOSED_IN_RX] = 1, the stop SI is SO_TX in a TX slot and EO_RX in an RX slot.
- 7) Coarse calibration stops autonomously.
- 8) The sensitivity of the ports for either TX, RX or both is programmable.

In addition, a bit called ALW_EN is associated with each block controlled by a DCF. Setting this bit to '1' activates the block irrespective of any other condition that causes the activation or deactivation of the DCF. All ALW_EN bits of the LMX4169 have been collected

in a single (18 bit!) register called ALW_EN_REG such that any combination of blocks or ports can be turned on or off with a single MICROWIRE™ transaction. The timing of DCFs is illustrated in Figure 4.

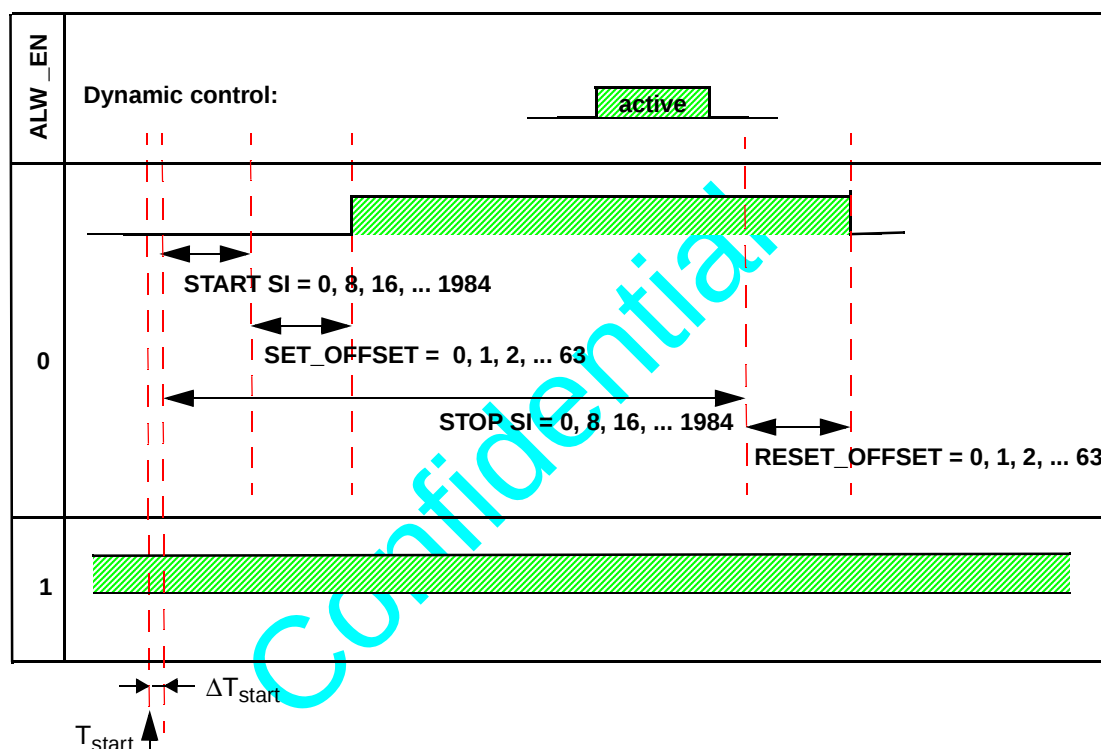


Figure 4 DCF timing

All times (in DECT bit periods) are counted with respect to a moment $T_{start} + \Delta T_{start}$, where T_{start} is the moment when a TX or RX setting in the BMCW was received (falling edge of LE) and ΔT_{start} is a delay related to the processing of the BMCW. There exists also a delay ΔT_{alw_en} from the moment of receiving ALW_EN_REG (falling edge of LE) until it results in activation or deactivation of a block (not shown in the figure). Characteristic values for these delays are listed in Table 54.

Port DCFs have two control bits instead of the DIS bit:

- EN_BY_TX: 'enable by transmit'; when '1', the sub-

block is activated in a TX slot'; the offsets are taken with respect to SO_TX and EO_TX.

- EN_BY_RX: 'enable by receive'; when '1', the sub-block is activated in an RX slot; the offsets are taken with respect to SO_RX and EO_RX.

Note that the combination of SIs and offsets allows to control block activation within a range of 0 to 2047 DECT symbol periods at a single symbol resolution. Controlling the blocks by programming ALW_EN_REG allows block activation with an arbitrary duration at a single symbol resolution but with the restriction that two consecutive changes are at least three symbols apart (when programming the MICROWIRE™ at maximal

speed, it takes three DECT symbols to transfer the 24 bits). The two mechanisms can be mixed at wish leading to a very flexible control of block activation.

4.4 FAST ANTENNA DIVERSITY

The LMX4169 has a special DCF for **fast antenna diversity** (FAD), the possibility to quickly switch between two available antennas. It is described in this section in conjunction with the behavior of the ports P0 and P0n that are dedicated for switching antennas. See document **National Semiconductor Application Note AN-D-100**: "LMX4169 Fast Antenna Diversity" for more information.

There are two moments relevant for the FAD algorithm:

- FAD_SWAP: the moment when the system starts measuring the strength of signal at the second antenna;
- FAD_DECIDE: the moment when the system selects the antenna with the strongest signal; the antenna that has been selected can be read from RSSI_REG[FAD_CHOICE].

These two moments are specified by a dedicated DCF, called FAD_WINDOW. Its settings are given by register FAD_WINDOW_DCF_REG (see Table 28). Its start-

and stop SIs are both defined from SO_RX (FAD_SWAP is a SET_OFFSET and FAD_DECIDE is a RESET_OFFSET). Whether the FAD algorithm should be activated, is given by the control bit SEL_FAD in the BMCW.

When FAD is to be used, and two antennas are therefore present, the following port connections need to be used:

- P1 controls the Rx switch
- P2 controls the Tx switch
- P0 controls Antenna 1
- P0n controls Antenna 2

In addition to the control bits already mentioned, there are two more that control the behavior of P0 and P0n:

- BURST_MODE_CTRL_REG[USE_ANTENNA2] to enforce the use of Antenna 2;
- PORT_CTRL_REG[ANT_INACTIVE_VAL] the output value when P0 or P0n are inactive.

The combination of control-bit settings leads to the behavior of P0 and P0n as given in Table 4.

Table 4: FAD and P0/P0n switching

SEL_FAD	USE_ANTENNA2	P0/P0n behavior
0	0	P0 follows P1 in RX slot and P2 in TX slot; P0n = ANT_INACTIVE_VAL.
0	1	P0 = ANT_INACTIVE_VAL P0n follows P1 in RX slot and P2 in TX slot.
1	don't care	If FAD_CHOICE = '0': P0 follows P1 in RX slot and P2 in TX slot; P0n = ANT_INACTIVE_VAL. If FAD_CHOICE = '1': P0 = ANT_INACTIVE_VAL P0n follows P1 in RX slot and P2 in TX slot. Note that FAD_CHOICE dynamically changes during an RX slot, resulting in the wanted FAD behavior.

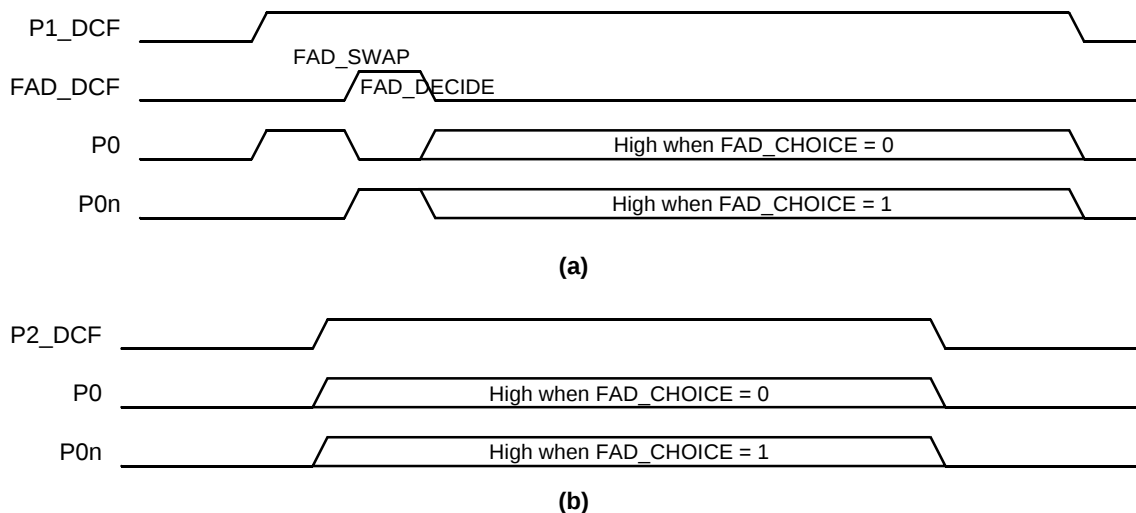


Figure 5 Example of typical timing of P0 and P0n when performing FAD: in an RX slot (a) and a TX slot (b)

A typical example of the behavior of P0 and P0n during an RX slot is shown in the timing diagram of Figure 5(a). For all signals, it is assumed that a DCF is high when active. As can be seen in the figure, the timing of P0 and P0n is derived from the DCFs of P1 and FAD_WINDOW. Figure 5(b) shows typical behavior in a TX slot where P0 and P0n only depend on the DCF of P2.

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5.0 Programming description

5.1 BURST MODE PROGRAMMING

Programming the BMCW will bring the LMX4169 in/out receive or transmit mode. For details, see chapter 4.2. The N COUNTER programming is described in Table 5

and 6 which enables the access of the DECT band for both reception and transmission.

The A counter value is programmed in PLL_N_CNTR[0:2] and the B counter value in PLL_N_CNTR[3:12].

Table 5: Receive mode N counter values

DECT channel	LO freq. [MHz] ¹⁾	Divider Ratio (N)	Counter values (Presc. = 8/9)	
			B [Dec.]	A [Dec.]
9	1882.656	2179	272	3
8	1884.384	2181	272	5
7	1886.112	2183	272	7
6	1887.840	2185	273	1
5	1889.568	2187	273	3
4	1891.296	2189	273	5
3	1893.024	2191	273	7
2	1894.752	2193	274	1
1	1896.480	2195	274	3
0	1898.208	2197	274	5

1) The LMX4169 is a so called 'lower-band' receiver

Table 6: Transmit mode N counter values

DECT channel	LO freq. [MHz]	Divider Ratio (N)	Counter values (Presc. = 8/9)	
			B [Dec.]	A [Dec.]
9	1881.792	2178	272	2
8	1883.520	2180	272	4
7	1885.248	2182	272	6
6	1886.976	2184	273	0
5	1888.704	2186	273	2
4	1890.432	2188	273	4
3	1892.160	2190	273	6
2	1893.888	2192	274	0
1	1895.616	2194	274	2
0	1897.344	2196	274	4

In receive mode, the RX bit must be '1' and a choice can be made how long the peak-hold function of the RSSI computation should be set. Normally, RSSI_STOP_AT_RX is '1' to indicate that the full slot is evaluated. When a quick evaluation of RSSI is required, RSSI_STOP_AT_RX is '0' to limit the time that peak-hold functionality is active.

In transmit mode the TX bit must be '1'.

In both receive and transmit mode, antenna diversity can be used. The functionality of SEL_FAD and USE_ANTENNA2 is described in paragraph 4.4.

5.2 IF CALIBRATION PROGRAMMING

Automatic calibration of the IF filter center frequency and bandwidth, and the IF amplifier DC offset voltage compensation can be performed. The IF calibration has to be performed only once after initial programming of the LMX4169. Afterwards the settings are kept in on-chip registers. Note that during calibration the reference clock should be present.

Before initiating IF calibration, the following conditions should be satisfied:

- RX_SI_REG[SO_RX_VAL] and RX_SI_REG[EO_RX_VAL] should have values unequal to zero;
- ALW_EN_REG[IF_ALW_EN] and ALW_EN_REG[ADC_ALW_EN] and ALW_EN_REG[DEM_ALW_EN] and ALW_EN_REG[BIAS_ALW_EN] should be set to '1';
- add a delay larger than 200 μ s before calibration to allow the IF section to settle.

IF calibration is initiated by making both RX and TX equal to '1' in the BMCW. This makes the system process a receive slot, but with a special behavior. At the start of the slot, the IF filter center frequency calibration procedure is executed. DC-offset calibration is done directly after that. The total time required is 432 DECT time units.

IF calibration should be terminated by making both RX and TX equal to '0' in the BMCW.

The IF_CAL_CAP value can be read back from the IF_CAL_REG register. This read back information can be used as a quantitative measure for the rate with which the calibration is to be repeated. The DC-offset values can not be read back.

5.3 AGC PROGRAMMING

The LMX4169 has a linear receive chain. All amplification is done by automatic gain control (AGC). The AGC is distributed within the receiver and consists of 4 variable gain amplifiers (VGAs). This distributed approach enables high sensitivity while preserving linearity in the presence of strong interference.

The settings of these amplifiers are controlled by the digital controller based on their associated signal level, or the received signal strength (RSSI). VGA0 is part of the LNA, VGA1 is situated before the IF filter, VGA2 before the ADC and VGA3 is a digital amplifier in the demodulator.

For AGC 1 through 3 the default settings give good results, AGC0 needs to be programmed since its performance is application dependent.

The gain setting of VGA1/2 and VGA3 are computed by comparison of the RSSI with 2 thresholds each, AGC12_TH_REG[AGC12_TH_HIGH], AGC12_TH_REG[AGC12_TH_LOW], AGC3_CTRL_REG[AGC3_TH_HIGH], AGC3_CTRL_REG[AGC3_TH_LOW] respectively.

When the RSSI rises over the higher threshold the

VGA is switched to a lower gain, while the gain is increased when the RSSI drops below the lower threshold. The settings of VGA1, 2 and 3 can be read back as

AGC_REG[GAIN_AGC1],
AGC_REG[GAIN_AGC2] and
AGC_REG[GAIN_AGC3] respectively.

VGA0 is implemented as a number of attenuators in the final stages of the LNA. The input impedance of the LNA remains constant, independent of the gain setting. The mutual influence of the attenuators is optimised such that the gain of the LNA is almost monotonous and linear with the gain setting (GAIN_AGC0), which can be programmed between 0x0 and 0xF, representing the lowest and highest value.

The value GAIN_AGC0 can not be programmed directly. It depends on the values of LNA_GAIN_REG[LNA_TST] and LNA_GAIN_REG[LNA_FXD].

The setting of LNA_TST determines which bits in GAIN_AGC0 are fixed (1) and which bits are controlled by AGC0 (0). For each bit in LNA_TST which value is 1, the gain is set by the corresponding bit in LNA_FXD. Constant gain is set by choosing LNA_TST=0xF. GAIN_AGC0 is then the same as LNA_FXD. For the bits in LNA_TST that are 0, the corresponding values in GAIN_AGC0 are toggled between 0 and 1 representing low and high gain values. The logical expression of the LNA gain is thus:

$GAIN_AGC0 = (LNA_TST \text{ AND } LNA_FXD) \text{ OR } (NOT(LNA_TST) \text{ AND } AGC0).$

All AND and OR operations are bitwise. The value of AGC0 should be interpreted as either 0xF for high gain or 0x0 for low gain. Some examples are given below.

GAIN_AGC0		LNA_TST	LNA_FXD
Fixed	1101	1111	1101
Auto	Low 0010 High 1011	0110	x01x

Since the setting of AGC0 depends on only one RSSI measurement, there is only one threshold (= LNA_GAIN_REG[TH_LNA]). The gain is measured in the time interval LNA Window with the DCF LNAW_DCF_REG. See document **National Semiconductor Application Note AN-D-102**: "LMX4169 LNA Automatic Gain Control" for more information.

Unlike AGC1/2/3, the gain of the LNA is not linear with its software setting. An approximate value of the gain difference between low and high must be accounted for in the computation of the RSSI value. This offset value can be determined during prototyping, by setting an RX input level between -80 and -50 dBm and programming GAIN_AGC0 fixed in the high gain value. Record the RSSI from RSSI_REG[RSSI_VAL]. Then program the GAIN_AGC0 fixed in the low gain value and vary RSSI_REG[LNA_RSSI] until the same RSSI value is read back.

6 On-Chip Registers

In this section first all registers that are present on the LMX4169, are summarized in Table 7. The entries in that table are grouped by function.

Next, each register is specified in detail in individual tables.

Table 7: Memory map of all on-chip registers

Address	Port	Description
0x00	BURST_MODE_CTRL_REG	BMCW
0x04	ALW_EN_REG	always-enable bits for block activation
0x08	PORT1_DCF_REG	Port 1 dynamic control function settings
0x09	PORT2_DCF_REG	Port 2 dynamic control function settings
0x0A	PORT3_DCF_REG	Port 3 dynamic control function settings
0x0B	PORT4_DCF_REG	Port 4 dynamic control function settings
0x10	EO_CAL_RSSI_REG	EO_CAL/EO_RSSI switch instant setting
0x11	TX_SI_REG	TX switch instant setting
0x12	RX_SI_REG	RX switch instant setting
0x20	PADRV_DCF_REG	PA driver dynamic control function
0x21	LNAMIX_DCF_REG	low-noise amplifier and mixer dynamic control function
0x22	LNAW_DCF_REG	LNA window dynamic control function
0x23	IF_DCF_REG	intermediate-frequency filter dynamic control function
0x24	ADC_DCF_REG	analog-to-digital converter dynamic control function
0x25	DEM_DCF_REG	demodulator dynamic control function
0x26	RSSIPH_DCF_REG	RSSI peak-hold computation dynamic control function
0x27	DBL_DCF_REG	frequency doubler dynamic control function
0x28	BIAS_DCF_REG	bias circuit dynamic control function
0x29	VCO_DCF_REG	voltage-controlled oscillator dynamic control function
0x2A	VCOCORE_DCF_REG	VCO core bias dynamic control function
0x2B	PLLCLOSED_DCF_REG	PLL closed loop dynamic control function
0x2C	COARSECAL_DCF_REG	coarse calibration circuitry dynamic control function
0x2D	VCOFILTER_DCF_REG	VCO core-bias-current filtering dynamic control function
0x2E	FAD_WINDOW_DCF_REG	fast antenna diversity dynamic control function
0x30	VCO_CTRL_REG	VCO control settings
0x31	PLL_CTRL_REG	PLL control settings
0x32	SYNTH_CTRL_REG	synthesizer control settings
0x33	PORT_CTRL_REG	port control settings
0x34	AGC_REG	automatic gain control read/write register
0x35	AGC12_TH_REG	AGC12 threshold settings
0x36	AGC12_ALPHA_REG	AGC12 envelope detection parameter
0x37	AGC3_CTRL_REG	AGC3 control settings
0x38	DEM_CTRL_REG	demodulator control settings
0x39	PREAMBLE_REG	preamble-processing control settings
0x3A	RSSI_REG	received-signal strength indication value
0x3B	LNA_GAIN_REG	LNA gain-stage settings

Table 7: Memory map of all on-chip registers

Address	Port	Description
0x3C	REF_OSC_REG	reference oscillator bits
0x3D	IF_CAL_REG	IF calibration settings
0x3E	PAD_IO_REG	disable digital inputs/outputs on digital pads
0x3F	TEST_MODE_REG	enable any of the digital test modes

6.1 REGISTER DESCRIPTIONS

Table 8: BURST_MODE_CTRL_REG (0x00)¹⁾

Bit	Mode	Symbol	Description	Reset
17	W	RX	Initiate a new receive slot after writing a '1'	0
16	W	TX	Initiate a new transmit slot after writing a '1'	0
15	W	USE_ANTENNA2	'0': use Antenna 1 '1': use Antenna 2	0
14	W	SEL_FAD	'0': do not use FAD '1': use FAD	0
13	W	RSSI_STOP_AT_RX	'0': use EO_RSSI as the Stop SI for RSSIPH '1': use EO_RX as the Stop SI for RSSIPH	0
12-0	W	PLL_N_CNTR	PLL N-counter value ²⁾	0

1) This register takes the address bits A[1:0] as extra data.

2) Bit 12 is reserved (not effective in current design), see paragraph 5.1.

Table 9: ALW_EN_REG (0x04)¹⁾

Bit	Mode	Symbol	Description	Reset
17	W	PADRV_ALW_EN	power-amplifier driver always enable	0
16	W	LNAMIX_ALW_EN	low-noise amplifier and mixer always enable	0
15	W	LNAW_ALW_EN	LNA window always enable	0
14	W	IF_ALW_EN	intermediate-frequency filter always enable	0
13	W	ADC_ALW_EN	analog-to-digital converter always enable	0
12	W	DEM_ALW_EN	demodulator always enable	0
11	W	RSSIPH_ALW_EN	RSSI peak-hold computation always enable	0
10	W	DBL_ALW_EN	frequency doubler always enable	0
9	W	BIAS_ALW_EN	bias circuit always enable	0
8	W	VCO_ALW_EN	voltage-controlled oscillator always enable	0
7	W	VCOCORE_ALW_EN	VCO core bias always enable	0
6	W	PLLCLOSED_ALW_EN	PLL closed loop always enable	0
5	W	COARSECAL_ALW_EN	coarse calibration circuitry always enable	0
4	W	VCOFILTER_ALW_EN	VCO core-bias-current filtering always enable	0
3	W	PORT1_ALW_EN	PORT1 always enable	0
2	W	PORT2_ALW_EN	PORT2 always enable	0
1	W	PORT3_ALW_EN	PORT3 always enable	0
0	W	PORT4_ALW_EN	PORT4 always enable	0

1) This register takes the address bits A[1:0] as extra data.

Table 10: PORT1_DCF_REG, PORT2_DCF_REG, PORT3_DCF_REG, PORT4_DCF_REG (0x08, 0x09, 0x0A, 0x0B)

Bit	Mode	Symbol	Description	Reset
13	W	EN_BY_RX	enable DCF in RX slot	0
12	W	EN_BY_TX	enable DCF in TX slot	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 11: EO_CAL_RSSI_REG (0x10)

Bit	Mode	Symbol	Description	Reset
15-8	W	EO_RSSI_VAL	End-of-RSSI switch instant value	0
7-0	W	EO_CAL_VAL	End-of VCO calibration switch instant activation value	0

Table 12: TX_SI_REG (0x11)

Bit	Mode	Symbol	Description	Reset
15-8	W	EO_TX_VAL	End-of-TX switch instant activation value	0
7-0	W	SO_TX_VAL	Start-of-TX switch instant activation value	0

Table 13: RX_SI_REG (0x12)

Bit	Mode	Symbol	Description	Reset
15-8	W	EO_RX_VAL	End-of-RX switch instant activation value	0
7-0	W	SO_RX_VAL	Start-of-RX switch instant activation value	0

Table 14: PADRV_DCF_REG (0x20)

Bit	Mode	Symbol	Description	Reset
13	W	RX_SENSITIVE	activate the DCF not only on TX but on RX as well	0
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 15: LNAMIX_DCF_REG (0x21)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 16: LNAW_DCF_REG (0x22)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 17: IF_DCF_REG (0x23)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 18: ADC_DCF_REG (0x24)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 19: DEM_DCF_REG (0x25)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 20: RSSIPH_DCF_REG (0x26)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 21: DBL_DCF_REG (0x27)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 22: BIAS_DCF_REG (0x28)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 23: VCO_DCF_REG (0x29)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 24: VCOCORE_DCF_REG (0x2A)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 25: PLLCLOSED_DCF_REG (0x2B)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 26: COARSECAL_DCF_REG (0x2C)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	-			0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 27: VCOFILTER_DCF_REG (0x2D)

Bit	Mode	Symbol	Description	Reset
12	W	DIS	disable DCF irrespective of its switch instants	0
11-6	W	RESET_OFFSET	offset w.r.t. stop switch instant	0
5-0	W	SET_OFFSET	offset w.r.t. start switch instant	0

Table 28: FAD_WINDOW_DCF_REG (0x2E)

Bit	Mode	Symbol	Description	Reset
11-6	W	FAD_DECIDE	moment when FAD algorithm makes a choice between either of the two antennas	0x0
5-0	W	FAD_SWAP	moment when the FAD algorithm starts measuring from second antenna	0x0

Table 29: VCO_CTRL_REG (0x30)

Bit	Mode	Symbol	Description	Reset
14	W	RF_CAL_DIS	Disable RF calibration and use the value in VCO_CTUNE field	0
13	W	VCO_PWR_SETTLE	VCO-power settling time: '0': 5 μ s '1': 10 μ s	0
12-7	R/W	VCO_CTUNE	Impose a preset value for the coarse calibration capacitance settings (write) or report the value of the automatic calibration (read)	0x20
6-3	W	VCO_ICORE_SET	preset value for VCO core current: "0000": 3.0 mA "0001": 6.0 mA "0011": 9.0 mA "0111": 12.0 mA "1111": 13.5 mA	0011
2	W	VCO_VMOD_1V	'0': normal operation '1': force Vmod to 1V	0
1	W	VCO_VTUNE_1V	'0': normal operation '1': force Vtune to 1V	0
0	W	VCO_EXTERNAL	'0': internal VCO '1': external VCO	0

Table 30: PLL_CTRL_REG (0x31)

Bit	Mode	Symbol	Description	Reset
15	W	PLL_CLOSED_IN_RX	'0': normal operation '1': keep PLL in "closed loop" in RX slot	0
14	W	PLL_CTR_RST_DIS	'0': normal operation '1': disable PLL counter reset when in open loop	0
13	W	TOGGLE_C_LOOP	'0': normal operation '1': enable transmission gate for closed loop toggling	0
12-6	W	PLL_R_CNTR	PLL R-counter value ¹⁾	0x18
5	W	PLL_CAL_MODE	'0': normal operation '1': use external Nclk input (pin Test_3) instead of prescaler output.	0
4	W	CP_EN	'0': CP in power down while PLL in tri-state '1': disable CP power down	1
3	W	CP_POLARITY	'0': negative '1': positive	1
2-0	W	CP_CURRENT	Charge pump current code: 000 100 μ A 010 or 100 950 μ A 001 or 110 1.8 mA 011 or 101 2.7 mA 111 3.5 mA	111

1) Bits 6 and 5 of this field are reserved (only 5 LSBs effective in current design).

Table 31: SYNTH_CTRL_REG (0x32)

Bit	Mode	Symbol	Description	Reset
5	W	RF_CLK_DIG_MODE	force the RF clock in digital mode, rather than the analog mode based on differential inputs (default).	0
4	W	CLK_OFF	switch off 10.368 MHz clock to PLL during open loop	0
3-0	W	BIAS_TRIM	Bandgap reference voltage trimming	0x8

Table 32: PORT_CTRL_REG (0x33)

Bit	Mode	Symbol	Description	Reset
4	W	ANT_INACTIVE_VAL	output value when P0/P0n inactive.	1
3	W	PORT4_INV	'0': PORT4 DCF on P4 pin; '1': inverted PORT4 DCF on P4 pin.	0
2	W	PORT3_INV	'0': PORT3 DCF on P3 pin; '1': inverted PORT3 DCF on P3 pin.	0
1	W	PORT2_INV	'0': PORT2 DCF on P2 pin; '1': inverted PORT2 DCF on P2 pin.	0
0	W	PORT1_INV	'0': PORT1 DCF on P1 pin; '1': inverted PORT1 DCF on P1 pin.	0

Table 33: AGC_REG (0x34)

Bit	Mode	Symbol	Description	Reset
12-9	R/W	GAIN_AGC3	gain value computed for AGC3 (read) or test value supplied externally (write); 0001: 21 dB 0010: 18 dB 0011: 15 dB 0100: 12 dB 0101: 9 dB 0110: 6 dB 0111: 3 dB 1000 and other values: 0dB	0001
8-5	R/W	GAIN_AGC2	gain value computed for AGC2 (read) or test value supplied externally (write); 1111: 28 dB 0111: 22 dB 0011: 16 dB 0001: 10 dB 0000: 4 dB	1111
4-2	R/W	GAIN_AGC1	gain value computed for AGC1 (read) or test value supplied externally (write); 111 27 dB 011 21 dB 001 15 dB 000 9 dB	111
1	W	AGC_PD_RESET	'0': AGC only reset by hardware reset '1': AGC also reset by demodulator power down	1
0	W	AGC_EXTERN	'0': VGA gains controlled by AGC '1': VGA gains provided externally	0

Table 34: AGC12_TH_REG (0x35)

Bit	Mode	Symbol	Description	Reset
15-8	W	AGC12_TH_HIGH	AGC12 hysteresis high threshold (switch down one step when exceeding this level)	0x73
7-0	W	AGC12_TH_LOW	AGC12 hysteresis low threshold (switch up one step when dropping below this level)	0x1A

Table 35: AGC12_ALPHA_REG (0x36)

Bit	Mode	Symbol	Description	Reset
5-0	W	AGC12_ALPHA	AGC12 envelope detection parameter (a higher value means a slower adaptation to input-level change)	0x38

Table 36: AGC3_CTRL_REG (0x37)

Bit	Mode	Symbol	Description	Reset
15-10	W	AGC3_ALPHA	AGC3 envelope detection parameter (a higher value means a slower adaptation to input-level change)	0x38
9-5	W	AGC3_TH_HIGH	AGC3 hysteresis high threshold (switch down one step when exceeding this level)	0x1D
4-0	W	AGC3_TH_LOW	AGC3 hysteresis low threshold (switch up one step when dropping below this level)	0x10

Table 37: DEM_CTRL_REG (0x38)

Bit	Mode	Symbol	Description	Reset
9	W	DEM_INVERT	'0': normal demodulator output '1': inverted demodulator output	0
8-2	R/W	SLICE_VAL	return measured slice value (read) or force fixed slice value (write)	0x0
1	W	SLICE_EN	'0': use slice value given by SLICE_VAL '1': use measured slice value	0
0	W	AGC_FREEZE	'0': AGC always active '1': freeze gain after preamble	0

Table 38: PREAMBLE_REG (0x39)

Bit	Mode	Symbol	Description	Reset
7-6	W	PREAMBLE_SYM	preamble averaging period necessary for frequency compensation: "00": 8 symbols "01": 12 symbols "10" or "11": 14 symbols	00
5-0	W	PREAMBLE_DEL	delay in symbols of start moment for frequency compensation, measured from enabling time of demodulator	0x0

Table 39: RSSI_REG (0x3A)

Bit	Mode	Symbol	Description	Reset
10-7	W	LNA_RSSI	Programmable gain difference between high and low gain of LNA [0..15] dB for RSSI computation. (Non-linear relationship with LNA_GAIN_REG settings)	0x0
6	R	FAD_CHOICE	The antenna chosen by the FAD algorithm: '0': Antenna 1 '1': Antenna 2	0x0
5-0	R	RSSI_VAL	RSSI value	0x0

Table 40: LNA_GAIN_REG (0x3B)

Bit	Mode	Symbol	Description	Reset
13-10	W	LNA_FXD	LNA gain setting when in fixed gain mode.	0x0
9-6	W	LNA_TST	Per bit switch between computed and fixed gain mode. '0': for bit position <i>i</i> : use AGC0 setting as GAIN_AGC0[<i>i</i>] '1': for bit position <i>i</i> : use fixed value, given by LNA_FXD[<i>i</i>] as GAIN_AGC0[<i>i</i>].	0x0
5-0	W	TH_LNA	Programmable threshold for LNA switching	0x0

Table 41: REF_OSC_REG (0x3C)¹⁾

Bit	Mode	Symbol	Description	Reset
15-7	W	CNT_CLK	number of clock pulses corresponding to the value of CNT_RO	0x07C
6-1	W	CNT_RO	number of reference oscillator periods that need to be counted	0x10
0	W	EXTERN_IF_CAL_CAP	'0': use capacitance value as determined by IF calibration for IF filter; '1': use the value written to IF_CAL_REG for IF filter.	0

1) In DAC test mode, bits 6-1 are used for DAC_TST_VAL.

Table 42: IF_CAL_REG (0x3D)

Bit	Mode	Symbol	Description	Reset
5-0	R/W	IF_CAL_CAP	IF calibration capacitance value; read the result of automatic calibration or write an external value	0x20

Table 43: PAD_IO_REG (0x3E)

Bit	Mode	Symbol	Description	Reset
15-8	W	PAD_SE_N	disable digital input on pads (MSB-LSB order is: P3, P2, P1, P0n, P0, <i>Test_3</i> , <i>Test_4</i> , P4).	0xFF
7-0	W	PAD_OE_N	disable digital output on pads (MSB-LSB order is: P3, P2, P1, P0n, P0, <i>Test_4</i> , <i>Test_3</i> , P4).	0xFF
15	W	P3_SE_N	disable digital input on pad P3	1
14	W	P2_SE_N	disable digital input on pad P2	1
13	W	P1_SE_N	disable digital input on pad P1	1
12	W	P0N_SE_N	disable digital input on pad P0n	1
11	W	P0_SE_N	disable digital input on pad P0	1
10	W	TEST3_SE_N	disable digital input on pad <i>Test_3</i>	1
9	W	TEST4_SE_N	disable digital input on pad <i>Test_4</i>	1
8	W	P4_SE_N	disable digital output on pad P4	1
7	W	P3_OE_N	disable digital output on pad P3	1
6	W	P2_OE_N	disable digital output on pad P2	1
5	W	P1_OE_N	disable digital output on pad P1	1
4	W	P0N_OE_N	disable digital output on pad P0n	1
3	W	P0_OE_N	disable digital output on pad P0	1
2	W	TEST4_OE_N	disable digital output on pad <i>Test_4</i>	1
1	W	TEST3_OE_N	disable digital output on pad <i>Test_3</i>	1
0	W	P4_OE_N	disable digital output on pad P4	1

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Table 44: TEST_MODE_REG (0x3F)^{1) 2)}

Bit	Mode	Symbol	Description	Reset
11-10	W	PLL_TST_MODE	PLL test mode (in LMX4168: PLL_TEST[1:0])	0
9	W	DAC_TST	'0': normal operation '1': put the value of DAC_TST_VAL (see REF_OSC_REG) on DAC input instead of the RSSI value.	0
8	W	PLL_TEST	'0': normal operation '1': connect PLL test-mode output (as defined by TEST_MODE_REG[PLL_TST_MODE]) to Pin Test3 and connect reference clock to Pin Test4.	0
7	W	RO_TO_PIN	when '1', enable the reference oscillator and connect its output to the RX_DATA output pin. The IF calibration value IF_CAL_REG[IF_CAL_CAP] will also be reset.	0
6	W	VOL	when '1', force all digital outputs to '0' (for production pad-driver test)	0
5	W	VOH	'0': Normal operation '1': force all digital outputs to '1' (for production pad-driver test)	0
4	W	ADC_TST	'0': normal operation '1': connect ADC output to pins P3, P2, P1, P0n, P0, Test_4, Test_3, P4 (MSB:LSB)	0
3	W	TGATE_IF_PIN	'0': normal operation '1': IF output/ADC input connected to pin P0 (Tgate[2] in 4168)	0
2	W	TGATE_MIXER_PINS	'0': normal operation '1': IF input to pins P3, P2, P1, P0n (Tgate[1] in 4168)	0
1	W	TGATE_MIXER_IF	'0': Mixer/IF disconnected '1': Mixer/IF connected (Tgate[0] in 4168)	1
0	W	SC_MODE	'0': Normal mode '1': Enable scan-test mode; this setting dominates any other test-mode.	0

1) Only one of PLL_TEST, VOL, VOH, ADC_TST is supposed to be '1' at the same time.

2) This table describes various test modes and will be removed in the final version of the datasheet.

7.0 Specifications

7.1 ABSOLUTE MAXIMUM RATINGS

Table 45: Absolute Maximum Ratings (Note 2)

Parameter	Description	Min	Typ	Max	Units
V _{dd} _{max}	Power Supply Voltage (V _{dd} _shield, V _{dd} _ADC, V _{dd} _mix, V _{dd} _LNA, V _{dd} _ESD, V _{dd} _PAdr, V _{dd} _presc, V _{dd} _PLL, V _{dd} _VCO, V _{dd} _bias, V _{dd} _dig, V _{dd} _RSSI)	-0.3	-	3.0	V
	Absolute difference between power supplies	-	-	0.3	V
V _n _{max}	Voltage on any pin	-0.3	-	V _{dd} +0.3	V
T _{storage}	Storage Temperature	-40	-	+150	°C
T _{Lead}	Lead Temp. (solder 4 sec) (Note 3)	-	-	+ 260	°C
V _{HBM}	ESD - human body model (Note 4)	-	-	2.0	kV
V _{MM}	ESD - machine model (Note 4)	-	-	100	V

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only to the test conditions listed.

Note 3: MSL 2 (Moisture Sensitivity Level) is valid when the standard reflow process (235°C) or leadfree reflow process (260°C) is used. MSL 2 means 1 year shelf life after opening dry-pack. Storage conditions are max. 30°C / 60% relative humidity.

Note 4: ESD STATEMENT

This device is a high performance RF integrated circuit and is ESD sensitive. Handling and assembly of this device should be performed at ESD free workstations.

7.2 ELECTRICAL CHARACTERISTICS

Electrical characteristics define the performance of the LMX4169 under the conditions as stated with the tables.

tbc: To Be Characterised, **tbd:** To Be Defined.

Table 46: Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Units
V _{dd}	Power Supply Voltage (V _{dd} _shield, V _{dd} _ADC, V _{dd} _mix, V _{dd} _LNA, V _{dd} _ESD, V _{dd} _PAdr, V _{dd} _presc, V _{dd} _PLL, V _{dd} _VCO, V _{dd} _bias, V _{dd} _dig, V _{dd} _RSSI)	2.4	2.5	2.6	V
V _{TXout}	PA driver output biasing voltage on pins TXoutZ, TXout	-	2.0	-	V
T _a	Operating ambient temperature	0	+25	+55	°C
R _{ref}	Reference resistor connected from pin 7 to Vss (see Table 1)	60.76	62	63.24	kΩ
f _{refClk}	Refer to CMOS digital input (see Table 51)	-	10.368	-	MHz

7.2.1 DC supply currents

The DC supply currents are defined into their respective supply pins, in a number of typical modes of operation (cases 1 through 8, see below). The currents are measured with the programming instructions where provided.

1. Power down current of all blocks combined, all blocks disabled, no reference clock applied;
2. Power down current of all blocks combined, all blocks disabled, with analog differential reference clock applied;
3. Power down current of all blocks combined, all blocks disabled, with digital reference clock applied;
4. During IF calibration;
TEST_MODE_REG = 0x0080
5. Synthesizer in closed loop, default VCO core current and charge pump settings, with analog differential reference clock applied;
(PLL in closed loop, VCO core enabled, VCO enabled, bias enabled, V_{tune} = 1V, V_{mod} = 1V)
ALW_EN_REG = 0x003C0
VCO_CTRL_REG = 0x101C
6. Receiver in open loop, default VCO core current settings, with analog differential reference clock applied;
(VCO core enabled, VCO enabled, bias enabled, doubler enabled, RSSI peak hold enabled, demodulator enabled, ADC enabled, IF enabled, LNA and mixer enabled, V_{tune} = 1V, V_{mod} = 1V)
ALW_EN_REG = 0x17F80
VCO_CTRL_REG = 0x501E
7. Same as case 6, however with digital reference clock applied and RSSI DAC enabled;
SYNTH_CTRL_REG = 0x0028
8. Transmitter in open loop, default VCO core current settings;
(VCO core enabled, VCO enabled, bias enabled, doubler enabled, PA driver enabled, V_{tune} = 1V, V_{mod} = 1V)
ALW_EN_REG = 0x20780
VCO_CTRL_REG = 0x501E

Table 47: DC Supply currents (Note 5)

Note 5: V_{dd} = 2.5 V, R_{ref} = 62 kΩ, 0°C ≤ T_a ≤ +55°C unless specified otherwise; Typical values for T_a = 25°C.

Note 6: Not tested, based on calculations of individual pin currents.

Parameter	Description	Condition	Min	Typ	Max	Units
Idd_PDN_1	total static current, without reference clock	case 1	-	0.001	0.02	mA
Idd_PDN_2	total static current, with analog differential reference clock applied	case 2	-	0.30	1	mA
Idd_PDN_3	total static current, with digital reference clock applied	case 3	-	0.30	1	mA
Idd_shield	current into Vdd_shield pin	cases 2, 3, 4, 5, 6, 7, 8	-	0	0.02	mA
Idd_ESD	current into Vdd_ESD pins	cases 2, 3, 4, 5, 6, 7, 8	-	0	0.02	mA
Idd_bias_4	current into Vdd_bias pin, during IF calibration	case 4	-	0.30	1	mA
Idd_bias_5	current into Vdd_bias pin, PLL in closed loop	case 5	-	0.40	1	mA
Idd_bias_6	current into Vdd_bias pin, receiver in open loop	cases 6, 7	-	0.50	1	mA
Idd_bias_8	current into Vdd_bias pin, transmitter in open loop	case 8	-	0.45	1	mA
Idd_VCO	current into Vdd_VCO pin, PLL in closed loop	cases 5, 6, 7, 8	-	13	15	mA
Idd_PLL	current into Vdd_PLL pin, PLL in closed loop	case 5	-	3.3	4	mA
Idd_presc	current into Vdd_presc pin, PLL in closed loop	case 5	-	6.4	7	mA
Idd_PAdr_6	current into Vdd_PAdr pin, receiver in open loop	cases 6, 7	-	10.4	12	mA
Idd_PAdr_8	current into Vdd_PAdr pin, transmitter in open loop	case 8	-	5.3	6	mA
Idd_mix	current into Vdd_mix pin, receiver in open loop	cases 6, 7	-	30.7	35	mA
Idd_LNA	current into Vdd_LNA pin, receiver in open loop	cases 6, 7	-	16.5	20	mA

Table 47: DC Supply currents (Note 5)

Note 5: $V_{dd} = 2.5\text{ V}$, $R_{ref} = 62\text{ k}\Omega$, $0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$ unless specified otherwise; Typical values for $T_a = 25^\circ\text{C}$.

Note 6: Not tested, based on calculations of individual pin currents.

Parameter	Description	Condition	Min	Typ	Max	Units
Idd_IF_4	current into Vdd_IF pin, during IF calibration	case 4	-	1.7	2	mA
Idd_IF_6	current into Vdd_IF pin, receiver in open loop	cases 6, 7	-	6.0	8	mA
Idd_ADC	current into Vdd_ADC pin, receiver in open loop	cases 6, 7	-	6.5	7	mA
Idd_RFCLK_2	current into Vdd_RFCLK pin, with analog differential reference clock applied	cases 2, 4, 5, 6, 8	-	0.3	1	mA
Idd_RFCLK_7	current into Vdd_RFCLK pin, receiver in open loop with RSSI DAC enabled	case 7	-	0.5	1	mA
Idd_dig_2	current into Vdd_dig pin, with analog differential reference clock applied	cases 2, 4, 8	-	0	1	mA
Idd_dig_3	current into Vdd_dig pin, with digital reference clock applied	case 3	-	0.30	1	mA
Idd_dig_5	current into Vdd_dig pin, PLL in closed loop	case 5	-	0.75	1	mA
Idd_dig_6	current into Vdd_dig pin, receiver in open loop	case 6	-	5.5	6	mA
Idd_dig_7	current into Vdd_dig pin, receiver in open loop and RSSI DAC enabled, with digital reference clock applied	case 7	-	5.8	7	mA
Idd_1	Total supply current in power down state, no reference clock applied (Note 6)	case 1	-	0.001	0.02	mA
Idd_2	Total supply current in power down state, with analog differential reference clock applied (Note 6)	case 2	-	0.3	3.1	mA
Idd_3	Total supply current in power down state, with digital reference clock applied (Note 6)	case 3	-	0.3	2.1	mA
Idd_4	Total supply current during IF Calibration, excluding digital algorithmic current (Note 6)	case 4	-	2.3	4	mA
Idd_5	Total supply current while PLL in closed loop (Note 6)	case 5	-	24.1	29	mA
Idd_6	Total supply current while receiver enabled with PLL in open loop (Note 6)	case 6	-	76.4	90	mA
Idd_7	Total supply current while receiver in open loop and RSSI DAC enabled, with digital reference clock applied (Note 6)	case 7	-	76.9	91	mA
Idd_8	Total supply current while transmitter enabled with PLL in open loop, including I_PAdr (see Table 49) (Note 6)	case 8	-	29.1	35	mA

7.2.2 Radio Receiver specification

Table 48: Receiver (Note 7)(Note 8)

Note 7: $V_{dd} = 2.5\text{ V}$; $R_{ref} = 62\text{ k}\Omega$; $0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$ unless specified otherwise; $BER \leq 1E-3$; Typical values for $T_a = 25^\circ\text{C}$.

Note 8: RF power is defined at the $50\text{ }\Omega$ receiver matching network input of reference board No. *tbd*.

Note 9: Not tested.

Note 10: see application note on matching *tbd*.

Note 11: Tests performed on DECT channel 0, 5 and 9.

Note 12: Analog RSSI is available on RFCLKm while RFclock is in digital mode.

Parameter	Description	Condition	Min	Typ	Max	Units
f_in	Receiver input frequency range		1880	-	1930	MHz
Z1_Rx	Receiver input impedance. Refer to the equivalent circuit in Table 1 (Note 9)(Note 10)	f = 1890 MHz	-	10-j152	-	Ω
Z2_Rx			-	135-j399	-	Ω
Z3_Rx			-	10-j164	-	Ω
P_Rx	Receiver sensitivity at room temperature (Note 11)	$T_a = 25^\circ\text{C}$	-	-96	-94	dBm
P_Rx_T	Receiver sensitivity, full temperature range (Note 11)	$0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$	-	-	-93	dBm
P_Rx_f	Receiver sensitivity, degraded by frequency offset (Note 11)	$-90\text{ kHz} \leq$ frequency offset $\leq +70\text{ kHz}$; $T_a = 25^\circ\text{C}$	-	-	-90	dBm
P_in	Receiver input power range	$T_a = 25^\circ\text{C}$	-	-	+13	dBm
IPL	Intermodulation performance level (TBR06-TC19) (Note 11)	$GAIN_AGC0 \leq 6$; $T_a = 25^\circ\text{C}$	-47	-	-	dBm
CI_0	Interferer performance (TBR06-TC16) (Note 11)	$Y = M$; $T_a = 25^\circ\text{C}$	-	7.5	9	dB
CI_1		$Y = M \pm 1$; $T_a = 25^\circ\text{C}$	-	-17	-13	dB
CI_2		$Y = M \pm 2$; $T_a = 25^\circ\text{C}$	-	-40	-34	dB
CI_3		any other DECT channel; $T_a = 25^\circ\text{C}$	-	-46	-40	dB
P_in_RSSI_min	lower limit of RSSI monotonous range	code 000000; $T_a = 25^\circ\text{C}$	-	-	-95	dBm
P_in_RSSI_max	upper limit of RSSI monotonous range	code 111111; $GAIN_AGC0 = 0$; $T_a = 25^\circ\text{C}$	-	-	-37	dBm
RSSI_res	RSSI resolution (Note 9)		-	2	-	dB/step
V_RSSI	RSSI output voltage (Note 9)(Note 12)	Load: C = 8.2pF	0.2	-	1.3	V

7.2.3 Radio Transmitter specification

Table 49: Transmitter (Note 13)(Note 14)

Note 13: $V_{dd} = 2.5\text{ V}$; $R_{ref} = 62\text{ k}\Omega$; $0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$ unless specified otherwise; Typical values for $T_a = 25^\circ\text{C}$.

Note 14: RF power is defined at the $50\text{ }\Omega$ transmitter matching network output of reference board No. *tbd*.

Note 15: Not tested.

Note 16: see application note on matching *tbd*.

Note 17: Tests performed on DECT channel 0, 5 and 9.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_out	Transmitter output frequency range		1880	-	1930	MHz
Z1_Tx	PA driver output impedance. Refer to the equivalent circuit in Table 1. (Note 15)(Note 16)	f = 1890 MHz	-	2.5-j152	-	Ω
Z2_Tx			-	522-j487	-	Ω
Z3_Tx			-	2.5-j152	-	Ω
P_Tx	Transmitter output power (Note 17)		0	2	4	dBm
P_VCO1_2	VCO fundamental suppression	$T_a = 25^\circ\text{C}$	-	-	-35	dBc
P_VCO3_2	VCO 3rd harmonic suppression	$T_a = 25^\circ\text{C}$	-	-	-40	dBc
I_PAdr	PA driver bias current. Refer to the equivalent circuit in Table 1.	$T_a = 25^\circ\text{C}$	9	10	11	mA

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7.2.4 Synthesizer specification

Table 50: Synthesizer (PLL, VCO) (Note 18)

Note 18: $V_{dd} = 2.5\text{ V}$; $R_{ref} = 62\text{ k}\Omega$; $0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$ unless specified otherwise; Typical values for $T_a = 25^\circ\text{C}$.

Note 19: Sideband noise power defined relative to peak output power P_{Tx} , while PLL is in closed loop.

Note 20: Not tested.

Note 21: V_{mod} input must be biased to a fixed DC level while the synthesizer is enabled and not modulated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_PD	Phase detector frequency (Note 20)		-	432	-	kHz
I_CPO_0	Absolute Charge Pump current (source/sink) Refer to register: PLL_CTRL_REG[CP_CURRENT]	$V_{CPO} = V_{dd}/2$; [2:0] = 0 0 0	<i>tbc</i>	0.10	<i>tbc</i>	mA
I_CPO_2		$V_{CPO} = V_{dd}/2$; [2:0] = 0 1 0	<i>tbc</i>	0.95	<i>tbc</i>	mA
I_CPO_6		$V_{CPO} = V_{dd}/2$; [2:0] = 1 1 0	<i>tbc</i>	1.8	<i>tbc</i>	mA
I_CPO_5		$V_{CPO} = V_{dd}/2$; [2:0] = 1 0 1	<i>tbc</i>	2.7	<i>tbc</i>	mA
I_CPO_7		$V_{CPO} = V_{dd}/2$; [2:0] = 1 1 1	<i>tbc</i>	3.5	<i>tbc</i>	mA
I_CPO_tol	Charge Pump current tolerance (Note 20)	$0.5 \leq V_{CPO} \leq V_{dd} - 0.5$	-	10	15	%
I_CPO_tri	Charge Pump leakage current (Note 20)	TRISTATE; $0.5 \leq V_{CPO} \leq V_{dd} - 0.5$		10	1000	pA
K_VCO	VCO conversion factor	$f = 1.9\text{GHz}$; $V_{tune} = V_{dd}/2$	17	20	23	MHz/V
V_tune	VCO tuning voltage		0.5		$V_{dd}-0.5$	V
K_mod	Modulation conversion factor	$f = 1.9\text{GHz}$; $V_{mod} = V_{dd}/2$	<i>tbc</i>	900	<i>tbc</i>	kHz/V
V_mod	VCO modulation voltage (Note 21)		0.5		$V_{dd}-0.5$	V
ACP_1	Adjacent Channel Power in $M \pm 1$ (Note 19)	$M = \text{ch5}$; RBW = 100 kHz; peak-hold; $T_a = 25^\circ\text{C}$	-	-	-95	dBc/Hz
ACP_2	Adjacent Channel Power in $M \pm 2$ (Note 19)	$M = \text{ch5}$; RBW = 100 kHz; peak-hold; $T_a = 25^\circ\text{C}$	-	-	-117	dBc/Hz
ACP_3	Adjacent Channel Power in $M \pm 3$ (Note 19)	$M = \text{ch5}$; RBW = 100 kHz; peak-hold; $T_a = 25^\circ\text{C}$	-	-	-128	dBc/Hz

7.2.5 Digital control specification

Table 51: CMOS digital input(Note 22)

Note 22: Vdd = 2.5 V; R_ref = 62 kΩ; 0°C ≤ T_a ≤ +55°C unless specified otherwise; Typical values for T_a = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{IH}	High level input voltage		0.7*Vdd	-	Vdd	V
V _{IL}	Low level input voltage		0	-	0.3*Vdd	V

Table 52: CMOS digital output(Note 23)

Note 23: Vdd = 2.5 V; R_ref = 62 kΩ; 0°C ≤ T_a ≤ +55°C unless specified otherwise; Typical values for T_a = 25°C.

Note 24: This resembles the worst case situation, when enabling a PA and four diode switches: P0n, P2, P3 and P4 sourcing currents; P0 and P1 disabled.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{OH}	High level output voltage	I _{out} = 2 mA	Vdd-0.5	-	Vdd	V
V _{OL}	Low level output voltage	I _{out} = 2 mA	0	-	0.5	V
I _{out}	Logic port output current for ports P0n and P2 (measured simultaneously)	TEST_MODE_REG = 0x0020; PAD_IO_REG = 0xFF2E; I[P3], I[P4] = 2 mA; V[P0n], V[P2] ≥ Vdd-0.5 (Note 24)	4	5	<i>tbc</i>	mA

Table 53: Microwire timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
tSK_setup	SIO to rising edge SK setup time in write mode		10	-	-	ns
tSK_hold	SIO to rising edge SK hold time in write mode		10	-	-	ns
tSIO_rd_valid	SIO valid after rising edge SK in read mode.		30	-	-	ns
tSK2LE	Rising edge SK to falling edge LE separation		15	-	-	ns
tLE2SK	Falling edge LE to rising edge SK separation		30	-	-	ns
fSK	SK frequency		-	-	20	MHz

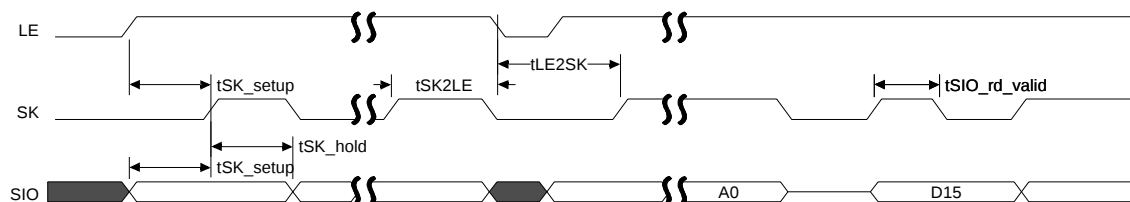

Figure 6 MICROWIRE™ signal-edge pairs used for timing specification.

Table 54: Digital Control

Symbol	Parameter	Condition	Min	Typ	Max	Units
tLE_start	Falling edge LE to active dynamic control function	LE for BMCW indicating start of burst	2.60	-	3.47	μs
tLE_ALW_EN	Falling edge LE to DCF activation/deactivation through ALW_EN	LE for ALW_EN_REG	0.00	-	0.90	μs

Table 55: RSTn Pin

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_low	Low time to reset device		10	-	-	μs

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8.0 Package Information

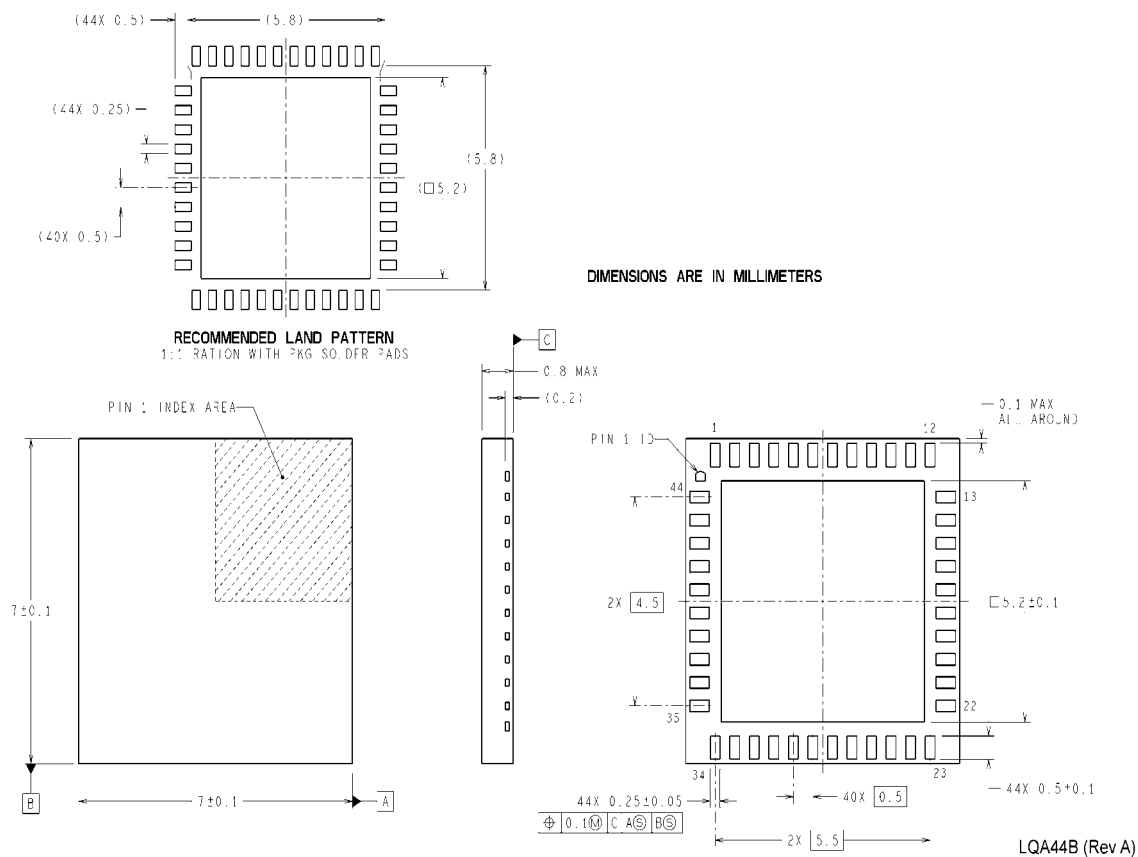


Figure 7 44 pins Leadless Leadframe Package. NS Package Number LQA044

Note 25: Refer to the application note AN-1187 for relevant soldering information.

This document can be downloaded from <http://www.national.com/an/AN-1187.pdf>

Product Status Definitions

Datasheet Status	Product Status	Definition
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